14-bit two-step successive approximation ADC with calibration circuit for high-resolution CMOS imagers

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A 14-bit two-step successive approximation analogue-to-digital converter (SA ADC) for high-resolution CMOS imagers is proposed. The proposed SA ADC consumes a small area because it uses only a capacitor array for 7-bit resolution to implement 14-bit ADC. To enhance accuracy, it uses digital-to-analogue conversion (DAC) embedded reference buffers to calibrate reference voltages. The average switching energy in the capacitor array is only 5.8 pJ per single conversion step. The HSPICE post-layout simulation results show that SNDR of the proposed ADC is improved from 73.41 to 81.52 dB after calibration.

Introduction: As new structures such as the mirrorless digital single-lens reflex camera (DSLR) are developed, the demands for CMOS imagers with a high-resolution format, high frame rate and high ADC resolution have rapidly increased. Single-slope (SS) ADCs have normally been used to achieve high-resolution because of their good linearity performance. However, SS ADCs in CMOS imagers having high-resolution pixel format such as DSLR use a very fast clock frequency of over a gigahertz [1]. The SS ADC increases power consumption and the design complexity of the counter and makes channel uniformity vulnerable to clock skew. Because cyclic and SA ADCs require relatively slow clock frequency around 10 MHz, they are good alternatives for high-resolution CMOS imagers [2, 3]. However, cyclic ADCs also consume a great amount of power because of the need for a high-gain analogue amplifier [2]. Although SA ADCs do not need an analogue amplifier with high power consumption, they require a large area of capacitors to generate the reference voltages for comparison operation [3] and this capacitor array increases power consumption from the reference buffers. It is also difficult to transfer accurate reference voltages owing to a large RC time constant. In this Letter, we propose a two-step SA ADC to reduce area and power consumption without decreasing ADC resolution.

Proposed two-step SA ADC: Fig. 1 shows the schematic diagram of the proposed two-step SA ADC. The operations are divided by sampling, coarse and fine AD conversions. When SW0 turns on in the sampling operation, all multiplexers (MUXs) select the output voltage \( V_{\text{REFP}} \) of a pixel circuit, and a capacitor array composed of \( C_0 \) to \( C_7 \) samples \( V_{\text{PIX}} \). When SW1 turns on and SW2 turns off, AD conversion starts. The upper seven bits \( D_7 \) to \( D_0 \) are resolved in coarse AD conversion. MUXs select a reference voltage \( V_{\text{REFP}} \), which is the full-scale reference, to generate the voltage for the bit decision, and they retain the \( V_{\text{REFP}} \) or return \( V_{\text{GND}} \) as the output of the comparator (CMP). After the coarse AD conversion, 1-bit data of each 2-bit latch is assigned to the upper seven bits. The attenuation capacitor \( C_i \) is used to reduce the area of the capacitor array. In the fine AD conversion, the proposed ADC uses \( V_{\text{REFP}} \) and \( V_{\text{REFN}} \) instead of \( V_{\text{REFP}} \) and \( V_{\text{GND}} \) to resolve the lower seven bits. \( V_{\text{REFP}} \) and \( V_{\text{REFN}} \) are provided by a reference generator, as will be explained below, and they are defined as

\[
V_{\text{REFP}} = V_{\text{REFP1}} + V_{\text{REFP2}}/2^7
\]

and

\[
V_{\text{REFN}} = V_{\text{REFP1}}/2^7
\]

In this period, MUXs select \( V_{\text{REFP2}} \) or \( V_{\text{REFN2}} \) according to the resolved upper seven digital bits \( D_{7-0} \) to \( D_{7-0} \) in the coarse step. When \( D_7 \) is logic ‘high’, for instance, MUX selects \( V_{\text{REFP2}} \) to generate the voltage for \( D_6 \) bit-decision. \( D_6 \) is determined as the output of the comparator. Depending on whether \( D_7 \) is logic ‘high’ or ‘low’, the output voltage of the MUX retains \( V_{\text{REFP2}} \) or returns to \( V_{\text{REFP1}} \) again, respectively. When \( D_7 \) is logic ‘low’, on the other hand, MUX selects \( V_{\text{REFN2}} \) and the same AD conversion operation is performed. After the coarse and fine AD conversion operations are finished, the output voltage \( (V_{\text{DAC}}) \) of the capacitor array digital-to-analogue converter (DAC) converges to the common-mode voltage \( (V_{\text{CM}}) \) and can be expressed as

\[
V_{\text{DAC}} = V_{\text{CM}} - V_{\text{REFP}} + \sum_{i=1}^{13} D_i \times V_{\text{REFP}} + \sum_{i=1}^{13} D_i \times V_{\text{REFN}}/2^7
\]

Proposed reference voltage calibration circuit: Even though the same capacitor array is used in the coarse and fine AD conversion operations, an error of the \( V_{\text{REFP2}} \) and \( V_{\text{REFN2}} \) causes errors of lower seven bits. The maximum error \( V_{\text{MAXERR}} \) of \( V_{\text{DAC}} \) can occur when the lower seven bits are all logic ‘high’. \( V_{\text{MAXERR}} \) is given by

\[
V_{\text{MAXERR}} = \frac{\sum_{i=0}^{6} \Delta_i (2^7 - 1) \times \Delta}{2^7} \approx \Delta
\]

where the magnitude of the reference voltage error is \( \Delta \). Therefore, the accuracy of the two additional reference voltages, \( V_{\text{REFP2}} \) and \( V_{\text{REFN2}} \), directly affects the ADC resolution. Fig. 2 shows a schematic diagram of the proposed reference voltage generator with a calibration circuit. The proposed reference generator uses analogue buffers embedding the DAC function to supply analogue voltages with 14-bit resolution of the ADC input range. The circuit block is composed of an error amplifier (AMP), a driving transistor \( (P1) \) and several resistors, and generates the input voltages of the analogue buffers (BUFS). BUF1 and BUF2 provide the accurate \( V_{\text{REFP2}} \) and \( V_{\text{REFN2}} \) to the two-step SA ADC by adjusting the transconductance \( (g_m) \) of the input transistors according to the digital 7-bit input, \( D_{\text{CAL-REFP}} \) and \( D_{\text{CAL-REFN}} \) [4]. The output of BUF \( (V_{\text{BUFOUT}}) \) can be expressed as

\[
V_{\text{BUFOUT}} = \sum_{i=0}^{5} D_i \times 2^i \times V_{\text{PHI}} + \sum_{i=0}^{5} D_i \times 2^i \times V_{\text{PHI}}
\]

Simulation results: Comparison results of the switching energy charging and discharging of the capacitor array for the conventional binary weighted capacitor, reference scaled [3], and the proposed two-step SA ADC are shown in Fig. 3. MATLAB simulation was performed assuming that three different type ADCs use the same conditions of 100 F\( \text{unit} \) capacitor \( (C_0) \) size and 2 V input range. Simulation results in Fig. 3 show that the average switching energy of the proposed

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Fig. 1 Schematic diagram of proposed two-step SA ADC

Fig. 2 Schematic diagram of proposed reference voltage generator with calibration circuit
two-step SA ADC is only 1.06% compared with that of the reference scaled SA ADC. Furthermore, the area of the capacitor array in the proposed two-step ADC is approximately 1/58 of that in the reference scaled SA ADC. Power reduction was achieved mainly through the reduced total area of the capacitor array and the use of a reduced reference voltage, $V_{REFN}$. The proposed two-step SA ADC and reference voltage generator were designed in a 0.13 μm CMOS process. The ADC was designed in 9 μm channel pitch accurately to extract the parasitic capacitance. For verification of the reference voltage generator with the DAC embedded analogue buffers, the HSPICE post-layout simulation for the proposed SA ADC was performed. After calibration, the simulated SNDR was enhanced from 73.41 to 81.52 dB, as shown in Fig. 4.

**Fig. 3** Switching energy of capacitor array against output code of SA ADC

**Fig. 4** Simulated FFT spectrum sampled at 375 kHz

Conclusions: A 14-bit two-step SA ADC is proposed for high-resolution CMOS imagers. The proposed two-step SA ADC is able to resolve 14-bit using only the capacitor array for 7-bit conversion and two additional reference voltages. As the area of the capacitor array reduces, the power consumption for driving the capacitor array reduces and the conversion rate increases. Simulation results show that the ADC error caused by the two additional reference voltages is also reduced using the DAC embedded reference buffers. Therefore, it is expected that the proposed two-step SA ADC is appropriate for high pixel and ADC resolution CMOS imagers.