A ΔΣ-cyclic Hybrid ADC for Parallel Readout Sensor Applications

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Abstract—In this paper, an ADC for parallel readout to convert large amount data in sensor applications is proposed. The ADC achieves small area and low power consumption by using two-step conversion. A 1st-order ΔΣ ADC converts coarse bits and then a cyclic ADC converts fine bits. An operational amplifier, comparators, capacitors, and switches used in the ADCs are efficiently shared to reduce power consumption and area. The proposed ADC has simple switching sequence, large tolerance to comparator offset and shared reference voltage between the coarse and fine ADCs. The designed circuit was fabricated in 0.18 μm CMOS using a 1.8 V supply voltage. It consumes 24 μW with 5 MHz clock speed. The measurement results show that SNR is varied from 47.89 to 57.58 dB according to the number of oversampling at 1st-order ΔΣ ADC.

I. INTRODUCTION

A column-parallel readout is used to process large amount of data for the massively parallel sensing systems such as CMOS imagers and DNA microarrays. An ADC in a column-parallel readout requires small area to be placed within narrow pitch, low power consumption, moderate conversion speed to convert large amount of data in short time, and high resolution to increase the dynamic range.

A single-slope ADC and successive approximation ADC are usually used in column parallel readout for low power consumption [1], [2]. However, the single-slope ADC requires very high speed clock to enhance the resolution of the ADC because it uses two times faster clock to increase the resolution by 1-bit. The successive approximation ADC needs a capacitor DAC consuming large area because it needs two times larger capacitor DAC to increase the resolution of by 1-bit.

In order to improve the conversion speed, area, and resolution of readout circuit, a cyclic ADC and ΔΣ ADC have been researched. A cyclic ADC for column-parallel readout was introduced in [3]. The cyclic ADC has an advantage of short conversion time because it needs the number of cycles as many as the A/D resolution bit. However, the cyclic ADC requires an operational amplifier with high gain and large sampling capacitors to reduce the gain error and sampling noise, respectively. For this reason, the cyclic ADC is normally used in applications requiring short conversion time and moderate A/D resolution. On the other hand, a ΔΣ ADC [4] can easily achieve high A/D resolution performance due to its noise shaping property. When the same resolution is required, the ΔΣ ADC can use smaller sampling capacitor than cyclic ADC because the sampling error from the thermal noise is averaged according to the number of oversampling. The required DC gain of an operational amplifier is also lower than the cyclic ADC. However, it requires relatively long conversion time because of the oversampling operation. For this reason, the ΔΣ ADC is usually used for applications requiring high A/D resolution and allowing long conversion time.

In order to overcome the disadvantages of the cyclic ADC and the ΔΣ ADC, the hybrid ADCs combining them were introduced in [5-6]. The ΔΣ ADC converts coarse bits to achieve high resolution by using oversampling operation and noise shaping property. Fine bits are converted by the cyclic ADC to reduce the conversion time. These hybrid ADCs share operational amplifier, comparators, capacitors, and switches between the ADCs to reduce power consumption and area. However, the hybrid ADC in [5] has complex switching sequence because the lots of switches are required to share the analog circuitries. Thus, they are not suitable for applications requiring small area readout circuit. The hybrid ADC in [6] is vulnerable to non-linearity error because the residue voltage of an operational amplifier after the ΔΣ ADC conversion process can be out of the conversion range of the cyclic ADC.

This paper presents a hybrid ADC composed of ΔΣ ADC and cyclic ADC which has simple switching sequence, large tolerance to comparator offset, and shared reference voltages between the ADCs.

II. ADC ARCHITECTURE

A. Proposed architecture

The block diagram of proposed hybrid ADC, which consists of a 1st-order ΔΣ ADC and a cyclic ADC, is shown in Fig. 1. The coarse bits (D_COARSE) are resolved by the 1st-order ΔΣ ADC. And the residue voltage (V_RES), which is the output voltage of an operational amplifier after the coarse conversion, is converted to fine bits (D_FINE) by the cyclic ADC.
D\textsubscript{COARSE} and D\textsubscript{FINE} are combined by an error correction logic to compensate offset error of the comparator [7]. The 1\textsuperscript{st}-order ΔΣ ADC and cyclic ADC share the analog such as an operational amplifier, comparators, capacitors, and switches to reduce power consumption and area. The operating sequence of the 1\textsuperscript{st}-order ΔΣ ADC for oversampling the input signal is illustrated in Fig. 2. The sampling capacitor (C1) and feedback capacitors (C2, C3) have same capacitance. At the first conversion cycle, the circuit operates as a sample and hold circuit. In the sampling phase, the C1 samples the input signal (V\textsubscript{IN}) and the C2 and C3 are reset. In the holding phase, the sampled signal in the C1 is transferred to the C2 and C3. The output voltage of an operational amplifier after the first conversion cycle is given by

\[ V_{OUT}[1] = V_{IN} / 2 \]  

After that, the 1\textsuperscript{st}-order ΔΣ ADC repeats the sampling and integrating process until the oversampling is finished. During the integrating phase, the DAC outputs +V\textsubscript{REF} or -V\textsubscript{REF} according to the output of the comparator, C\textsubscript{COARSE} (+1 or -1). At the last conversion cycle, the 1\textsuperscript{st}-order ΔΣ ADC samples the common voltage (V\textsubscript{CM}) instead of the input signal. In the integrating phase, the reference voltage (+V\textsubscript{REF} or -V\textsubscript{REF}) is only integrated to the feedback capacitors. After the last cycle, the sampling number of the input signal and the reference voltage becomes equal. When the 1\textsuperscript{st}-order ΔΣ ADC oversamples the input signal N times, the V\textsubscript{RES} of an operational amplifier after the 1\textsuperscript{st}-order ΔΣ ADC conversion process (V\textsubscript{OUT}[N+1]) can be expressed as

\[ V_{OUT}[N+1] = \frac{1}{2} \sum_{i=1}^{N} (V_{IN} - C_{COARSE}[i] \cdot V_{REF}) \]  

The V\textsubscript{OUT}[N+1] is resolved by the cyclic ADC. Operating sequence of the cyclic ADC in the hybrid ADC is described in Fig. 3. The C3 used in the 1\textsuperscript{st}-order ΔΣ ADC is disconnected from the input node of an operational amplifier. The operation of the cyclic ADC for converting 1.5-bits in each cycle is same in [3]. In the sampling phase, the C1 samples the output of an operational amplifier. In the amplifying phase, the sampled signal and reference voltage (+V\textsubscript{REF}, V\textsubscript{CM} or -V\textsubscript{REF}), which is selected by the comparator output, C\textsubscript{FINE} (+1, 0, or -1) are transferred to the C2. The output of an operational amplifier after the M+1\textsuperscript{th} amplifying phase (V\textsubscript{OUT}[M+1]) can be expressed as

\[ V_{OUT}[M+1] = 2 \cdot V_{OUT}[M] - C_{FINE}[M] \cdot V_{REF} \]  

The cyclic ADC repeats the sampling and amplifying operations during the A/D conversion cycles.

**B. Residue voltage after the 1\textsuperscript{st}-order ΔΣ ADC conversion**

The residue voltage of an operational amplifier after the 1\textsuperscript{st}-order ΔΣ ADC conversion process is plotted in Fig. 4. The 1\textsuperscript{st}-order ΔΣ ADC oversamples the input signal four times. The residue voltage is in a half of the ΔΣ ADC input range by using two times larger feedback capacitor than sampling.
capacitor. And then, the residue voltage is converted by the cyclic ADC. The cyclic ADC has same input range as $\Delta\Sigma$ ADC by using same reference voltages and disconnecting feedback capacitor, C3 used in $\Delta\Sigma$ ADC. The different reference voltages and capacitance mismatch can cause the large DNL and INL errors at the coarse bit transition point. To alleviate these errors, the hybrid ADC is designed to have same reference voltage between $\Delta\Sigma$ ADC and cyclic ADC. However, careful layout is still required to reduce the capacitance mismatch.

The residue voltage in a half of the cyclic ADC input range brings large tolerance for the comparator offset. When the comparator has the offset voltage, the residue voltage of an operational amplifier shifts vertically as much as the comparator offset. When the magnitude of comparator offset is smaller than a 1/4 of the ADC input range, non-linearity errors from the comparator offset are eliminated because the residue voltage is still in the resolvable range of the cyclic ADC. Thus, the proposed hybrid ADC is much insensitive to the comparator offset compared with the hybrid ADC in [6].

### III. CIRCUIT IMPLEMENTATION
The 1<sup>st</sup>-order $\Delta\Sigma$ ADC and cyclic ADC were implemented using a switched capacitor circuit as shown in Fig. 5. To reduce the area of a column parallel readout circuit with narrow pitch, the capacitors in ADC should have small capacitance. The C1, C2, and C3 have same capacitance of 50 fF. However, small capacitance increases capacitance mismatch and the sampling noise. At least, the capacitance mismatch should be under 0.1% to achieve 10-bit resolution. We optimized the layout using post layout simulation. The sampling noise is reduced by oversampling operation in the $\Delta\Sigma$ ADC. In our design, the hybrid ADC has the input voltage range of 0.8 V<sub>pk-to-pk</sub>. Although a typical nyquist rate ADC needs over 80 fF to achieve 10-bit resolution, the hybrid ADC using four times oversampling requires only 20 fF. Accordingly, the sampling and feedback capacitors of 50 fF are enough to 10-bit resolution. A two-stage operational amplifier is used in the hybrid ADC. In order to achieve 10-bit resolution and 5 MHz operation, the operational amplifier has the DC gain of 70 dB and the unity-gain bandwidth of 30 MHz. The simple structure of ADC is required to implement the hybrid ADC within narrow pitch of 7 μm. Comparing with hybrid ADC in [5], the number of control signals is reduced from 15 to 8, the number of switches is reduced from 24 to 11, and the number of unit capacitors is reduced from 5 to 3.

### IV. EXPERIMENTAL RESULTS
The proposed hybrid ADC was fabricated in 1P6M 0.18 μm process. A chip micrograph is shown in Fig. 6. The analog core occupies area of 7 μm × 175 μm. The digital block for the low pass filter and the error correction logic occupy area of 7 μm × 950 μm.

In order to evaluate the performance of the proposed ADC, the number of oversampling in the 1<sup>st</sup>-order $\Delta\Sigma$ ADC varied from 4 to 64 and the cyclic ADC converts the residue voltage for 8 cycles. The operating clock frequency of the hybrid ADC is fixed in 5 MHz and the conversion time is varied with the number of oversampling. A sine wave with 50 Hz and 0.8 V<sub>pk-to-pk</sub> is applied to the hybrid ADC to measure the SNDR and SNR. We used the sine wave with low frequency to reduce the distortion of the signal from varied on-resistance of a sampling switch. The FFT spectrum of ADC outputs with 4
Figure 6. Die photo of the proposed ADC. The proposed ADCs are arrayed to test for column-parallel readout.

Figure 7. Measured FFT spectrum of ADC outputs with number of oversampling, 4 and number of cycles for cyclic ADC, 8. ($F_{\text{in}}=50$ Hz, $F_{\text{s}}=50$ kHz)

![FFT Spectrum](image)

Table I. Measured SNDR and SNR with respect to the number of oversampling.

<table>
<thead>
<tr>
<th>Number of oversampling</th>
<th>SNDR [dB]</th>
<th>SNR [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>44.80</td>
<td>47.89</td>
</tr>
<tr>
<td>8</td>
<td>49.16</td>
<td>51.50</td>
</tr>
<tr>
<td>16</td>
<td>52.68</td>
<td>54.41</td>
</tr>
<tr>
<td>32</td>
<td>55.26</td>
<td>56.62</td>
</tr>
<tr>
<td>64</td>
<td>55.77</td>
<td>57.58</td>
</tr>
</tbody>
</table>

times oversampling is shown in Fig. 7. The measured SNDR and SNR are 44.80 and 47.89 dB, respectively. Table I shows the SNDR and SNR with respect to the number of Oversampling. As the number of oversampling doubles, the noise power is reduced to a half due to the oversampling operation. As a result, the SNR is improved by 3 dB whenever the number of oversampling doubles. The measured DNL and INL are $+1.40/-0.56$ and $+2.20/-4.00$ LSB as shown in Fig. 8 when the number of oversampling is 4 and the number of cycles for cyclic ADC is 8. The DNL error is increased at the coarse bit transition point. This is due to capacitance mismatch between the sampling capacitor and feedback capacitors. The error by capacitance mismatch can be alleviated by careful layout.

The total power consumption is 24 $\mu$W which consists of the power consumption of analog circuitry, 16 $\mu$W and digital block, 8 $\mu$W.

V. CONCLUSIONS

The proposed hybrid ADC converts coarse and fine bits using the 1st-order $\Delta\Sigma$ ADC and the cyclic ADC, respectively. It has advantages for simple switching sequence, large tolerance to the comparator offset. The power consumption is only 16 $\mu$W for analog circuitry and 8 $\mu$W for digital block. The ADC achieves SNR from 47.89 to 57.58 dB with respect to the number of oversampling from 4 to 64 times.

REFERENCES