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M2L-B Analog-to-Digital converters (Lecture)
Room: Vergina
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M2L-B.1 Design Of A 7-Bit 1GSPS Folding-Interpolation A/D Converter With Self-Calibration Technique
Younghoon Kim, Joongwon Jun, Kyuik Cho, Daeyun Kim, Joonho Moon, Minkyu Song

M2L-B.2 Calibration Of High-Resolution Flash Adcs Based On Histogram Test Methods
Armin Jalili Sebarden, Jacob Wikner, Sayed Masoud Sayedi, Kent Palmkvist, Mark Vesterbacka,

M2L-B.3 Pseudorandom Sequence Generation For Mismatch Analog Compensation Of Adcs
Victor R Gonzalez-Diaz, Edoardo Bonizzoni, Franco Maloberti

M2L-B.4 A Low-Power 12-Bit 2nd-Order S-/D Analog-To-Digital Converter For Cmos Image Sensors
Gun-Hee Yun, Min-Kyu Kim, Jong-Boo Kim, Min-Seok Shin, Oh-Kyong Kwon,

M2L-B.5 A Fully Digital Calibration Technique For Nonlinearity Correction In Pipelined Adcs
Tohid Moosazadeh, Mohammad Yavari
A Low-Power 12-bit 2nd-Order Σ-Δ Analog-to-Digital Converter for CMOS Image Sensors

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Abstract—A low-power and 12-bit resolution 2nd-order Σ-Δ ADC for CMOS image sensors is proposed. The proposed Σ-Δ ADC adopts the built-in correlated double sampling (CDS) technique and single-ended signaling to reduce the power consumption and chip area. The proposed Σ-Δ modulator of the ADC has the oversampling ratio (OSR) of 130 to achieve 12-bit resolution and the sampling rate of 10 MHz to complete analog-to-digital conversion within 13 μs. The proposed ADC has been implemented using 0.35 μm 1P4M standard CMOS process. The simulation results using HSPICE show 75.8 dB SNDR and 210 μW power consumption under 2.8 V supply voltage.

Keywords—CMOS Image Sensor; Σ-Δ Modulator; Column-Parallel Readout; Correlated Double Sampling; Analog-Digital Converter

I. INTRODUCTION

CMOS image sensors for medical, scientific, or high-end video applications require a high resolution ADC over 12 bit [1,2]. Σ-Δ ADCs easily archive high-resolution because they have noise shaping and oversampling properties [3]. However, the oversampling technique consumes large power because it needs a high-speed analog amplifier for high sampling rate.

Recently, several research results have been reported to reduce the power consumption of the Σ-Δ ADC for CMOS image sensors. Previous Σ-Δ ADCs should use an additional analog CDS amplifier or a digital CDS technique [4,5]. The analog CDS amplifier must require one or more high-performance operational amplifiers to reduce the sampling error [4]. In the digital CDS technique, Σ-Δ ADCs should have two times conversion rate [5]. Therefore, previous Σ-Δ ADCs consume large amount of power. They also use differential signaling to achieve low signal distortion and high noise immunity. However, Σ-Δ ADCs with differential architecture increase power consumption and chip area because they need two times number of capacitors and switches.

This work presents the 12-bit 2nd-order modified Σ-Δ modulator with the built-in CDS operation and single-ended architecture for low power consumption. The proposed 2nd-order Σ-Δ modulator samples reset and signal voltages from pixels. The CDS operation is automatically performed during charge transfer operation of the Σ-Δ modulator.

II. PROPOSED 2ND-ORDER Σ-Δ MODULATOR

A. System Overview

The proposed 2nd-order Σ-Δ modulator is designed for the HDTV resolution of 1920 × 1080 pixels and the operating speed of 60 frames per second. The row line time is 15.4 μs and the light integration time is 16.7 ms.

The conventional readout circuit of CMOS image sensors consists of the analog CDS amplifier and the Σ-Δ ADC as shown in Fig. 1(a). The pixel output is directly connected to the analog CDS amplifier. The analog CDS amplifier performs noise cancellation and pixel output voltage sampling [4]. In order to reduce the sampling error, it requires a high gain amplifier and large sampling capacitors. Thus, the analog CDS amplifier consumes lots of current. On the other hand, the readout circuit using the digital CDS technique does not need the analog CDS amplifier in Fig. 1(a) [5]. However, an ADC using the digital CDS technique consumes two times larger current than the ADC which uses the analog CDS amplifier because it requires two times of the normal operating speed.
In the proposed Σ-Δ ADC, the analog CDS amplifier is replaced by the input buffer circuit, as shown in Fig. 1(b). The input buffer circuit, which consists of a capacitor and two source-followers, stores the reset voltage of the pixel and drives the output capacitive load of the modulator’s input stage. This architecture reduces the power consumption and chip areas because two source followers consume much smaller current than the analog CDS amplifier.

The proposed Σ-Δ modulator uses the conventional 2nd-order cascaded integrators with distributed feedback (CIFB) structure and low power analog sub-circuits [3,6]. The size of capacitors and switches of the modulator are optimized to reduce the power consumption.

B. Circuit Operation

The circuit diagram of the proposed 2nd-order Σ-Δ modulator and the timing diagram of the pixel circuit are shown in Fig. 2 and Fig. 3, respectively. The proposed circuit uses the 4-transistor pixel structure with the photodiode (PD).

In the 4-transistor pixel structure, charges which generated by the incident light are integrated to the PD during frame time except one row-line time. RS and RT signals are high to turn on the reset transistor (T1) and the row-select transistor (T4) in the row-line time. The voltage of the floating diffusion (FD) becomes VDD and the reset voltage of the pixel (Vrst) is sampled to the Crst through the source follower (T3), T4, and the switch Sr. The input stage of the modulator samples Vrst through the source follower (SF2). When RT signal becomes low and TX signal becomes high, integrated charges in the PD are transferred to the FD. The input of the source follower (SF2) follows the integrated optical signal voltage of the pixel (Vsig). Transferred charges drop the potential of the cathode of the photodiode (PD).

The Σ-Δ modulator does not operate until the output voltage of the SF1 (Vsig_is) is completely settled to the final voltage level. The proposed Σ-Δ modulator uses two source followers to prevent the charge leakage and the capacitive coupling from clock switching operations. The timing diagram of the pixel circuit and the proposed modulator for the row line time is shown in Fig. 4. First of all, the D flip-flop and sampling capacitors of the Σ-Δ modulator are initialized when the rst signal becomes high. This initialization operation is essential to remove residue charges of feedback capacitors in the previous analog-to-digital conversion step because the residue charge causes an error of the output result.

After the initialization operation, the Σ-Δ modulator samples the level-shifted voltage of the Vrst (Vrst_is) and the adjust voltage (Vadj) to the Csla and the Cslb capacitor. At the phase Φ1, stored charges in Csla (Qcsla) and stored charges in Cslb (Qcslb) can be expressed as

\[ Q_{csla} = C_{sla} \cdot (V_{cm} - V_{rst}_{ls}) \]  

and

\[ Q_{cslb} = C_{slb} \cdot (V_{cm} - V_{adj}) \]  

respectively. At the phase Φ2, each voltage of the bottom plates in Csla and Cslb becomes Vsig_is and the reference voltage (Vref) which is the output voltage of the DAC in the Σ-Δ modulator. Vref voltage becomes Vrefp or Vrefn when the D flip-flop is high or low, respectively. Top plates of capacitors Csla and Cslb are connected to the negative input terminal of the operational amplifier (A1). Stored charges Qcsla and Qcslb are transferred to the feedback capacitor Cf1.
As a result, \( Q_{C2a} \) change of the output voltage in \( AI(V_{01}) \) is given by

\[
\Delta V_{(II)} = \frac{C_{S1a}}{C_{f1}}(V_{ns, b} - V_{sig, b}) + \frac{C_{S1b}}{C_{f1}}(V_{adj} - V_{ref}). \tag{3}
\]

Although the input common-mode voltage of the modulator should be \( V_{cm} \), the common-mode voltage of the input signal is different with \( V_{cm} \) because the output voltage in the pixel is changed with respect to the process and temperature variations. In order to solve this problem, \( V_{adj} \) should be expressed as

\[
V_{adj} = V_{cm} - \frac{V_{signal\_range}}{2}, \tag{4}
\]

where \( V_{signal\_range} \) is the voltage range of \( V_{sig} \).

The 2nd stage of the proposed \( \Sigma \Delta \) modulator performs the same operation of the conventional one [3]. \( V_{01} \) sampled to \( C_{2a} \) in the phase \( \Phi 2 \). The bottom plate of \( C_{2a} \) becomes to \( V_{cm} \) and the top plate of \( C_{2a} \) is connected to the negative terminal of second amplifier (\( A2 \)) in the phase \( \Phi 1 \). Sampled charges are transferred to the feedback capacitor (\( C_{\Phi 2} \)). The reference voltage \( V_{ref} \) is transferred to the feedback capacitor \( C_{\Phi 2} \) using \( C_{2b} \) as likes as the charge transfer operation of the \( V_{01} \) voltage. Total charges \( \langle Q_{C2} \rangle \) transferred from \( C_{2a} \) and \( C_{2b} \) to \( C_{\Phi 2} \) is given by

\[
Q_{C2} = C_{s2a} \cdot (V_{01}) - C_{s2b} \cdot (V_{ref}), \tag{5}
\]

and the output voltage of the 2nd stage can be expressed as

\[
\Delta V_{O2} = \frac{C_{s2a}}{C_{f2}}(V_{01}) - \frac{C_{s2b}}{C_{f2}}(V_{ref}). \tag{6}
\]

A clocked comparator (Comp) senses the output voltage of the second integrator [3]. A D-flip flop (D-\( FF \)) samples the output of the comparator.

C. Circuit Implementation

The proposed \( \Sigma \Delta \) modulator is implemented using single-ended CIFB structure, as shown in Fig. 2. The single-ended modulator reduces the number of capacitors and interconnection lines. As a result, it also reduces the power consumption.

The sampling capacitors \( C_{1s} \) and \( C_{2a} \) are 40 fF and 150 fF, respectively. \( C_{s2b} \) is 30 fF to generate one fifth of \( V_{ref} \) voltage. The feedback capacitors \( C_{f1} \) and \( C_{f2} \) are 200 fF and 320 fF, respectively. All capacitors are designed using the metal-insulator-metal (MIM) capacitor because the matching property among them is very important. The condition to minimize the sampling capacitor size is given by

\[
C_{S1a} = C_{S1b} = \frac{kT}{\text{OSR} \cdot (10^{\text{SNDR}/10} \cdot V^2_{\text{input\_range}} \cdot 0.5)}, \tag{7}
\]

where \( k, T, \text{SNDR} \) are the Boltzman constant, the absolute temperature, and the signal-to-noise and distortion ratio, respectively [3]. The size of feedback capacitors is determined so that the output voltage of the amplifier ranges from \( V_{refp} \) to \( V_{refn} \). \( Crst \) is several pF and is implemented by the MOS capacitor. Performance of the modulator is not sensitive to the accuracy of \( Crst \) because \( Crst \) only keeps the same voltage level during the modulator operation.

Two amplifiers in the modulator are designed by the conventional two-stage operational amplifier in [6] with PMOS input pair. The amplifiers are tightly designed to reduce power consumption. Each source follower of the input buffer consumes only the static current of 2 \( \mu \)A. Amplifiers of the 1st and 2nd stage consume 15 \( \mu \)A and 10 \( \mu \)A, respectively.

III. SIMULATION RESULTS

The proposed \( \Sigma \Delta \) modulator for CMOS image sensor applications was implemented in 1P4M 0.35 \( \mu \)m standard CMOS process. Fig. 5 shows the digital fast Fourier transform result of the proposed 2nd-order \( \Sigma \Delta \) modulator outputs. The baseband signal frequency is 76.9 kHz. Total static current of this circuit is only 29 \( \mu \)A under 2.8 V supply voltage. The baseband signal frequency is 76.9 kHz. Total static current of this circuit is only 29 \( \mu \)A under 2.8 V supply voltage. Fig. 6 represents simulation results of monotonic property in the proposed \( \Sigma \Delta \) ADC. Simulation was performed in various reset voltages of the pixel because it can be changed by the process and temperature variations. Fig. 6 shows that the proposed \( \Sigma \Delta \) ADC keeps monotonic property when the reset voltage of the pixel is shifted from 2.0 V to 1.8 V. In order to stabilize the operation of the 2nd-order \( \Sigma \Delta \) modulator, the input voltage range of the ADC should be less than the difference between \( V_{refp} \) and \( V_{refn} \) [3]. Thus, we used 1.6 V difference between \( V_{refp} \) and \( V_{refn} \) for 0.8 V input range. Therefore, the input voltage range can be expressed by 12-bit digital value when the 2nd-order \( \Sigma \Delta \) modulator outputs 13-bit digital value, as shown in Fig. 6. Simulation results using HSPICE of the proposed \( \Sigma \Delta \) modulator are summarized in Table I. The figure-of-merit (FOM) comparing with previously published column-parallel \( \Sigma \Delta \) ADCs is described in Table 2. The FOM is defined as

\[
\text{FOM} = \frac{\text{Power consumption}}{V_{\text{supply}}^2 \cdot 2^\text{ENOB} \cdot 2f_{\text{seg}}}. \tag{8}
\]
The FOM of the proposed Σ-Δ modulator is only 0.210 pJ/conversion-step. As a result, the proposed circuit shows three times performance enhancement compared with the Σ-Δ modulator in [7]. These results are obtained by comparing only the Σ-Δ modulator. The power consumption of the Σ-Δ ADC with the built-in CDS operation is reduced to about 58 percent of the conventional Σ-Δ ADC using the digital CDS technique and 52 percent of the conventional Σ-Δ ADC with the analog CDS operation.

IV. CONCLUSIONS

A low-power 12-bit 2nd-order Σ-Δ ADC with the built-in CDS operation for CMOS image sensors proposed. The proposed circuit performs the CDS operation and the analog-to-digital conversion, simultaneously. The proposed circuit uses single-ended signaling and optimizes the size of capacitors to reduce power consumption. Simulation results show that FOM of the proposed circuit is enhanced to 0.210 pJ/conversion-step. This enhancement is three times of previous circuits. Therefore, the proposed Σ-Δ ADC is appropriate for high-resolution CMOS image sensor applications.

Table I. Simulation Results of the Proposed Circuit

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Frequency (kHz)</td>
<td>8.5</td>
</tr>
<tr>
<td>Signal Bandwidth (kHz)</td>
<td>76.9</td>
</tr>
<tr>
<td>Sampling Frequency (kHz)</td>
<td>10.0</td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>75.8</td>
</tr>
<tr>
<td>Power Dissipation (µW)</td>
<td>132.0</td>
</tr>
<tr>
<td>Power Supply Voltage (V)</td>
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</tr>
<tr>
<td>ENOB (bit)</td>
<td>12.1</td>
</tr>
</tbody>
</table>

Table II. Comparison of Column-Parallel Σ-Δ Modulators for CMOS Image Sensors

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>[7]</td>
<td>11.2</td>
<td>150</td>
<td>50</td>
</tr>
<tr>
<td>[8].A</td>
<td>11.5</td>
<td>210</td>
<td>26</td>
</tr>
<tr>
<td>[8].B</td>
<td>13.0</td>
<td>270</td>
<td>17</td>
</tr>
<tr>
<td>[9]</td>
<td>12.0</td>
<td>1300</td>
<td>200</td>
</tr>
<tr>
<td>This work</td>
<td>12.1</td>
<td>132</td>
<td>77</td>
</tr>
</tbody>
</table>

Figure 5. Output spectrum of the proposed Σ-Δ modulator.

Figure 6. Digital output code of the proposed Σ-Δ modulator with a digital filter with respect to the reset voltage.

REFERENCES