P-16: A Scan Driver Circuit Using Transparent Thin Film Transistors

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Abstract
In this paper, we proposed two types of integrated scan driver circuits using only n-channel zinc-oxide (ZnO) thin film transistors (TFTs). One is the scan driver circuit for low-power consumption and the other scan driver is for robustness to threshold voltage and mobility variation. The proposed scan driver for low-power consumption is embedding level shifter and its power consumption was 1.4 mW. The scan driver for robustness used positive feedback circuits as pull-up devices. By simulation results, the proposed scan driver has robustness in the frequency, temperature, and process variation compared to conventional scan drivers. Also, two proposed scan drivers have advantages of full swing output range for VDD to VSS.

1. Introduction
Transparent electronics have attracted considerable interest because they can offer new applications for consumer electronics, transportation and business. Among them, thin film transistors (TFTs) on display backplane would be the most attractive. Therefore, there are researches to develop new materials for the active layer of transparent thin film transistors. Among the transparent semiconductor, zinc-oxide (ZnO) film has been used as an active channel material in exhibiting n-channel semiconductor characteristics with high optical transmittance in the visible region and wide band gap of 3.3 eV. In particular, the ZnO TFTs are of great interest due to their potential to replace hydrogenated amorphous silicon (a-Si:H) or polycrystalline silicon (poly-Si) TFTs because of good compatibility with a-Si:H TFT’s process and higher field-effect mobility than a-Si:H TFT. Moreover, ZnO TFTs have the advantage of low temperature process less than 200°C. So far, there have been promising reports for the high performance ZnO TFTs with moderate field effect mobility and high on/off ratio for the next generation display applications.

The n-channel TFTs of ZnO are made easier than p-channel TFTs due to its native defects such as interstitials zinc and vacancies of oxygen [1]. Thus, only n-channel circuits are available to make the circuits with ZnO TFTs. When circuits are designed only with n-channel transistors, the bootstrapping effects are used to overcome the limitation of n-channel TFTs [2–6]. However, the circuits using bootstrapping effect causes high power dissipation because static current occur when pull-down switches are turn on. The reason is that remained charge in the bootstrapping capacitors make pull-up devices turn on when pull-down devices turn on, and direct path occur from VDD to VSS. Furthermore, the bootstrapping effect is often failed due to threshold voltage variations that make sometimes TFTs depletion mode devices.

The phenomenon is caused by many excess carriers in the active layer of ZnO without gate-source voltage [7]. So, the research is needed to reduce power consumption and to design against threshold voltage variations.

In this paper, we proposed two types of scan drivers using only n-channel ZnO TFTs. The proposed low-power scan driver is made to improve power efficiency and embedded level shifter. The proposed robust scan driver is designed to overcome the threshold voltage variations and it use positive feedback.

2. Proposed Scan Drivers

2.1. Low-power Scan Driver
In Figure 1, TFTs of N1–N5 are for generating and shifting scan signals line by line in rows. TFTs of N6–N8 are used for the buffer with bootstrapping capacitance. VST is a start signal or the driver’s output of previous row, and VRST is a reset signal or the driver’s output of next row. When VST is VDD (20 V), the initial voltage of VRST is VSS (0 V) and the voltage on the node A becomes nearly 20 V. The clock signal, CLK, which is in the same phase of the start signal, VST, maintains the voltage on the node B as VSS. At the same time, the output voltage is discharged to VSS through N8. When VST and CLK go low, N2 is turned off. Then, the voltage on the node B increases, and node A is bootstrapped due to the parasitic capacitance between the gate and source node of N5. Without transistor N4, the charge is remained in the parasitic capacitance between node A and B. The remained charge cannot be discharged and N5 is not turns off when N2 turns on. The direct path is generated and power dissipations occur. So, N4 makes the voltage on node A be VDD + VTH so that the static current N5-N2 is reduced and power dissipation is reduced. Figure 2 shows timing diagram and Figure 3 shows block diagram of the proposed low-power scan driver.

![Figure 1. The schematic diagram of the low-power scan driver with embedding level shifter.](image-url)
2.2. Robust Scan Driver to Threshold Voltage Variation

Most conventional scan driver circuits with only n-channel TFTs are designed as a single stage building block to get the benefits from the bootstrapping effect with diode connected TFTs and capacitors like circuits in [2–6]. In using the bootstrapping effect, the remained charge in bootstrapping capacitors can be the reason of power dissipation and can limit output voltage range. More considerable problem of the bootstrapping effect is that it does not work with depletion-mode devices because diode connected TFTs become loss its function as a diode. Consequently, conventional circuits designed by using single channel TFTs in [2–6] are not applicable to oxide TFTs that have the characteristics shown as Figure 4.

Figure 5 shows the circuit and block diagrams of the proposed robust scan driver. The proposed scan driver consists of an input stage, a storage stage, and a buffer stage as shown Figure 5(a). The input circuit receives previous scan driver’s signals and puts the signals into the storage circuit after a half clock. Also, it prevents the output fluctuation due to the clock signal and it makes output stable. The storage circuit stores and transfers high or low signals to the buffer. The buffer receive signals from the storage circuit and drives large resistive and capacitive loads. The buffer also masks the signals to separate so that the scan signals are not overlapped and data of the pixels do not interfere between each row. The operation of the proposed scan driver is divided to two cases. The first case is when a previous row scan signal is VDD (20 V) and the second case is when a previous row scan signal is VSS (0 V). In the first case, four steps are defined by timing as shown Figure 6. In step 1, when a previous scan driver’s output becomes VDD, N2 is turned on and the node A increases to VDD. At that time, N1 and N4 are turned off because IN1 is VSSL (-10 V) and N3 is turned on by node A. N5 and N6 are turned on by IN4 which is VDD. N7 is turned off and N8 is turned on by N3. The current flows through N8, N10, and N11 due to high IN2 and IN3. In step 2, when IN3 is VSS, N11 is turned off and the voltage of the node B increases. At that time, the voltage of the node C does not increase because N9 is turned on. Next, in step 3, IN4 becomes VSS and N5 and N6 are turned off so that the input stage and the storage stage are isolated. Then the change of the input stage does not interfere with the storage stage and the scan driver’s output. In step 4, IN2 becomes VSSL and N9 is turned off, the parasitic capacitance of node C is charged and the voltage on node C increases. Node C turns N12 on and voltage of node B that is gate node of N10 increase. These operations are positive feedback between N10 and N12. These TFTs maintain the node C, node B, and output voltage. Finally N14 and N16 are turned on and OUT(n) becomes 20V to drive pixels in a row in the display panel. When previous scan signal maintains VSS, N1 is turned on synchronizing with the clock signal, CLK, which is induced to IN1. Node A is maintained by N1 continuously connecting VSS and node A. Therefore, N3 and N8 are turned off. On the other hand, when N1 is turned on, N4 is simultaneously turned on by IN1. Node D becomes high voltage and it makes N7 turn on so that node C is set as 0 V. If node C is high voltage, it makes N14 and N16 turn on if then OUT(n) becomes high voltage. So, it is important to size the input stage circuits and N7 because when pixels are not selected by the circuits, OUT(n) must be VSS. Figure 5 (b) shows relationship between clocks(CLK, CLKA, and CLKC) and inputs(IN1–IN4), CLKB, CLKAB, and CLKCB are shifted as a half clock phase.

3. Simulation Results

The simulations in this paper are conducted by modeling parameters extracted from ZnO TFTs. The parameters based on measurement data from 40μm×20μm ZnO TFTs at temperature 25°C. The field effect mobility is 5.27 cm²/V·s and S-slope is 252.6 mV/dec.
Figure 7 shows the output waveforms and the scan signals are generated sequentially. Figure 8 shows the power consumption of the proposed low-power scan driver with various supply voltages. We compared power consumptions of the proposed structure with previous reported shift register with embedding level shifter, which is proposed by B. S. Bae et al. [2] at \( V_{DD} \) is 20V without loads. Bae’s shift register can be compared with the proposed scan driver because it is also embedding level shifters and using bootstrapping effect. We can confirm that the proposed scan driver consumes 1.4mW and Bae’s shift register consumes 11.7mW [2].

The simulation is conducted for 7-inch VGA (640×480) resolution and for driving pixels in the AM-OLED display panels. The simulation of proposed robust scan driver is also considering depletion mode TFTs in circuits and pixels. To turn off absolutely some transistors in the scan drivers and pixels, we define that \( V_{SS} \) is -5 V and input voltage range is from -10 V to 10 V. Power consumption is 10.1 mW when \( V_{ON} \) is -2 V and 9.8 mW when \( V_{ON} \) is 0.5 V. \( V_{ON} \) is the voltage when \( I_{DS} \) starts increasing abruptly as shown Figure 4. These results of power consumption are so high comparing to scan drivers using other devices such as a-Si:H and p-Si, however pseudo inverter using ZnO TFTs consumed power as about 23 mW in the same conditions. Additionally in this condition the pseudo inverter is simple structure but the pseudo inverter is bigger than the proposed scan driver. The values obtained from simulation results are abnormal compared to the work with a-Si:H, p-Si and c-Si. However proposed scan drivers are improved when comparing conventional circuits made of the same material. Figure 9 shows successfully operate at 16.7 kHz for VGA resolution with 100pF load capacitance and resistance calculated for 7 inch AM-OLED panels.

### 4. Conclusions

This work proposed two types of proposed scan drivers. The proposed low-power scan driver with embedding level shifter and consumed 0.8–3.6 mW at 15–30 V. The proposed robust scan driver is verified that can operate in stable when the threshold voltages caused by process and temperature variations are varied from -3 V to 1 V by the simulation. The scan drivers can apply to AM-OLED displays.

### 5. Acknowledgements

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**Table 1. Simulation conditions.**

<table>
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<tr>
<th>Panel size</th>
<th>7 inch</th>
<th>Resolution</th>
<th>VGA</th>
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<td>Load capacitance (pF)</td>
<td>100</td>
<td>Load Resistance (KΩ)</td>
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<td>Frame rate (Hz)</td>
<td>60</td>
<td>Input voltage (V)</td>
<td>-10 ~ 10</td>
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<tr>
<td>( V_{SS} ) (V)</td>
<td>20</td>
<td>( V_{SS} ) (V)</td>
<td>-5</td>
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6. References


